Amendments to the Claims:

This listing of claims will replace all prior versions of the claims in the present application:

Listing of Claims:

1. (Currently Amended) A phase offset cancellation circuitry comprising:

at least two phase detectors for receiving component clock signals of a multi-phase clock generator, wherein at least some of the clock signals are offset from each other, each of the at least two phase detectors for detecting phase differences between pairs of component clock signals, wherein each of the at least two phase detectors measures a phase spacing of adjacent component clock signals;

at least one summer coupled to the at least two phase detectors for measuring the phase differences between the at least two phase detectors, wherein the at least one summer includes:

a mirror circuit coupled to the at least two phase detectors for detecting a difference between the outputs of the at least two phase detectors;

a capacitor coupled to the mirror circuit for charging or discharging based upon the phase difference; and

at least one variable delay element for receiving the measured phase differences and for providing a delay which is proportional to an output value of the at least one summer, wherein the delay is used to reduce the phase difference between pairs of component clock signals.

2. (Cancelled)

3. (Original) The system of claim 1 wherein each of the at least two phase detectors comprise:

a current source; and

two switches coupled to the current source, the two switches receiving a first and a second component clock signal, wherein when the two switches are closed the phase detector generates an indication of the difference between the first and second clock signals.

4. (Cancelled)

5. (Original) The system of claim 1 wherein the each of the at least two phase detectors provides a voltage as an output.

6. (Original) The system of claim 1 wherein the each of the at least two phase detectors provides a current as an output.

7. (Original) The system of claim 1 wherein each of the at least two phase detectors are calibrated to minimize device mismatch within the phase detector.

8. (Currently Amended) A multi-phase clock generator comprising:

a plurality of clocks for clocking input data;

a plurality of samplers coupled to the plurality of [[docks]]clocks for receiving the input data, each of the samplers receiving a different clock phase; and

a phase offset cancellation system coupled to the plurality of clocks, the phase offset cancellation system further comprising a plurality of phase detectors for receiving component clock signals of the multi-phase clock generator, wherein at least some of the clock signals are offset from each other, each of the plurality of phase detectors for detecting phase differences between pairs of component clock signals;

wherein each of the plurality two phase detectors measures a

phase spacing of adjacent clocks;

at least one summer coupled to the two phase detectors for measuring the phase differences between the at least two phase detectors; and at least one variable delay element for receiving the measured phase differences and for providing a delay which is proportional to an output value of the at least one summer, wherein the at least one summer includes:

a mirror circuit coupled to the at least two phase detectors for detecting a difference between the outputs of the at least two phase detectors; and

a capacitor coupled to the mirror circuit for charging or discharging based upon the phase difference, wherein the delay is used to reduce the phase difference between pairs of component clock signals.

9. (Cancelled)

10. (Original) The multi-phase clock generator of claim 8 wherein each of the at least two phase detectors comprise:

a current source; and

two switches coupled to the current source, the two switches receiving a first and a second clock phase, wherein when the two switches are closed the phase detector generates an indication of the difference between the first and second clock phases.

11. (Cancelled)

12. (Original) The multi-phase clock generator of claim 8 wherein the each of the at least two phase detectors provides a voltage as an output.

13. (Original) The multi-phase clock generator of claim 8 wherein the each of the at least two phase detectors provides a current as an output.

14. (Original) The multi-phase clock generator of claim 8 wherein each of the at least two phase detectors are calibrated to minimize device mismatch within the phase detector.

15. (Currently Amended) A system for use with a multi-phase clock generator comprising:

a plurality of phase detectors coupled to the multiphase clock generator for receiving clock phases from the multi-phase clock generator, wherein each of the phase detectors measures a phase spacing of adjacent clocks; and

at least two phase detectors for receiving component clock signals of a multi-phase clock generator, wherein at least some of the clock signals are offset from each other, each of the phase detectors for detecting phase differences between pairs of component clock signals;

at least one summer coupled to the at least two phase detectors for measuring the phase differences between the at least two phase detectors, wherein the at least one summer includes:

a mirror circuit coupled to at least two phase detectors for detecting a difference between the outputs of the at least two phase detectors;

a capacitor coupled to the mirror circuit for charging or discharging based upon the phase difference; and

at least one variable delay element for receiving the measured phase differences and for providing a delay which is proportional to an output value of the at least one summer, wherein the delay is used to reduce the phase difference between pairs of component clock signals.

16. (Original) The system of claim 15 wherein each of the plurality of phase detectors comprises:

a current source; and

two switches coupled to the current source, the two switches receiving a first and a second clock phase, wherein when the two switches are

closed the phase detector generates an indication of the difference between the first and second clock phases.

17. (Cancelled)

18. (Original) The system of claim 17 wherein each of the at least two phase detectors are calibrated to minimize device mismatch within the phase detector.

19. (Currently Amended) A circuit comprising:

a multi-phase clock generator; and

phase offset cancellation circuitry, coupled to the multi-phase clock generator, the phase offset cancellation circuitry further comprising at least two phase detectors for receiving component clock signals of a multi-phase clock generator, wherein at least some of the clock signals are offset from each other, each of the phase detectors for detecting phase differences between pairs of component clock signals, wherein each of the at least two phase detectors measures a phase spacing of adjacent component clock signals;

at least one summer coupled to the two phase detectors for measuring the phase differences between the at least two phase detectors, wherein the at least one summer includes:

a mirror circuit coupled to the at least two phase detectors for detecting a difference between the outputs of the at least two phase detectors;

a capacitor coupled to the mirror circuit for charging or discharging based upon the phase difference; and

at least one variable delay element for receiving the measured phase differences and for providing a delay which is proportional to an output value of the at least one summer, wherein the delay is used to reduce the phase difference between pairs of component clock signals.

20. (Currently Amended) A system comprising:

means for generating a multi-phase clock; and

means for cancelling phase offsets in the multi-phase clock, the phase offset cancelling means comprising at least two phase detectors for receiving component clock signals of a multi-phase clock generator, wherein at least some of the clock signals are offset from each other, each of the phase detectors for detecting phase differences between pairs of component clock signals, wherein each of the at least two phase detectors measures a phase spacing of adjacent component clock signals;

at least one summer coupled to the two phase detectors for measuring the phase differences between the at least two phase detectors, wherein the at least one summer includes:

a mirror circuit coupled to the at least two phase detectors for detecting a difference between the outputs of the at least two phase detectors;

a capacitor coupled to the mirror circuit for charging or discharging based upon the phase difference; and

at least one variable delay element for receiving the measured phase differences and for providing a delay which is proportional to an output value of the at least one summer, wherein the delay is used to reduce the phase difference between pairs of component clock signals.

21. (Currently Amended) A transmitter comprising:

a multi-phase clock generator;

phase offset cancellation circuitry for cancelling phase offsets of the multi-phase clock generator, the phase offset cancellation circuitry being coupled to the multi-phase clock generator, the phase offset cancellation circuitry further comprising at least two phase detectors for receiving component clock signals of a multi-phase clock generator, wherein at least some of the clock signals are offset from each other, each of the phase detectors for detecting phase differences between pairs of component clock signals, wherein each of the at least two phase detectors measures a phase spacing of adjacent component clock signals;

at least one summer coupled to the two phase detectors for measuring the phase differences between the at least two phase detectors, wherein the at least one summer includes:

a mirror circuit coupled to the at least two phase detectors for detecting a difference between the outputs of the at least two phase detectors;

a capacitor coupled to the mirror circuit for charging or discharging based upon the phase difference;

at least one variable delay element for receiving the measured phase differences and for providing a delay which is proportional to an output value of the at least one summer, wherein the delay is used to reduce the phase difference between pairs of component clock signals; and

a driver that is clocked by the phase offset cancelled multi-phase clock generator.

22. (Currently Amended) A receiver comprising:

a multi-phase clock generator;

phase offset cancellation circuitry for cancelling phase offsets of the multi-phase clock generator, the phase offset cancellation circuitry being coupled to the multi-phase clock generator, the phase offset cancellation circuitry further comprising at least two phase detectors for receiving component clock signals of a multi-phase clock generator, wherein at least some of the clock signals are offset from each other, each of the phase detectors for detecting phase differences between pairs of component clock signals, wherein each of the at least two phase detectors measures a phase spacing of adjacent component clock signals;

at least one summer coupled to the two phase detectors for measuring the phase differences between the at least two phase detectors, wherein the at least one summer includes:

a mirror circuit coupled to the at least two phase detectors for detecting a difference between the outputs of the at least two phase detectors;

a capacitor coupled to the mirror circuit for charging or discharging

based upon the phase difference; and

at least one variable delay element for receiving the measured phase differences and for providing a delay which is proportional to an output value of the at least one summer, wherein the delay is used to reduce the phase difference between pairs of component clock signals; and

a sampler that is clocked by the phase offset cancelled multi-phase clock generator.

23. (Currently Amended) A system comprising:

a multi-phase clock generator;

a receiver coupled to the multi-phase clock generator;

a transmitter coupled to the multi-phase clock generator; and

phase offset cancellation circuitry for cancelling phase offsets of the multi-phase clock generator, the phase offset cancellation circuitry being coupled to the multi-phase clock generator, the phase offset cancellation circuitry further comprising at least two phase detectors for receiving component clock signals of a multi-phase clock generator, wherein at least some of the clock signals are offset from each other, each of the phase detectors for detecting phase differences between pairs of component clock signals, wherein each of the at least two phase detectors measures a phase spacing of adjacent component clock signals;

at least one summer coupled to the two phase detectors for measuring the phase differences between the at least two phase detectors, wherein the at least one summer includes:

a mirror circuit coupled to the at least two phase detectors for detecting a difference between the outputs of the at least two phase detectors;

a capacitor coupled to the mirror circuit for charging or discharging based upon the phase difference; and

at least one variable delay element for receiving the measured phase differences and for providing a delay which is proportional to an output value of the at least one summer, wherein the delay is used to reduce the phase

difference between pairs of component clock signals, wherein the transmitter and/or receiver utilize the phase offset cancelled multiphase clock generator.